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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,738	04/02/2004	Mark G. Barmettler	4100-00200	1386

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EXAMINER	
PHAM, BRENDA H	

ART UNIT	PAPER NUMBER
2416	

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01/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,738	BARMETTLER, MARK G.	
	Examiner	Art Unit	
	BRENDA PHAM	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/31/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *13-28* is/are withdrawn from consideration.

5)☒ Claim(s) *6-12* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Andrews et al (US 5,572,695).

Regarding claim 1, Andrews et al discloses an adapter channel mapping system for mapping channels of a network, comprising (referring to FIG. 4):

a memory component **(memories 52)** operable to communicate with the network and having a first memory portion **(Channel work area 58, "logical 2k area 58")** and a second memory portion **(Channel data area 60, "logical 8k memory area 60")**, the first memory portion operable to communicate with a first physical channel of the network corresponding to at least a first cabling wire and the second memory portion operable to communicate with a second physical channel of the network corresponding to at least a second cabling wire **(In mode 2, each DSP can share the first and second memory pages (e.g., 128K words) in the DRAM. The first and second logical lookup addresses are independently mapped to either one of the first and second lookup regions. The first and second logical channel work addresses are**

independently mapped to any one of the eight physical channel areas in the first and second channel work regions. The first and second logical channel addresses are independently mapped to any one of the eight physical channel areas in the first and second channel regions." Col. 4, lines 32-43); and

a mapping component **(LOOKUP 1, LOOKUP 2 of DRAM memory 54)** operable to map each one of the first and second memory portion **(Channel work area 58 and Channel data area 60)** to one of the first and second physical channels **("one of the eight physical channel areas in the first and second channel work regions")** based on a first configuration **(Mode 1 address mapping is shown in FIG. 4 by the solid lines between the logical DSP addresses 52 and the first 64K page 55 of DRAM addresses. In mode 1, each DSP shares only the first 64K page 55 of memory 54. Accordingly, there is only one lookup section 64 is mapped into the first ligcal 21.75k area 56 of each DSP's memory range 52. The four channel work area 68 are mapped into the next logical 2k area 58 while the four channel areas 70 are mapped into the last logical 8K memory area 60" col. 8, lines 42-51)** of the network and further operable to map each of the first and second memory portions to one of the first and second physical channels based on a second configuration of the network **("Mode 2 address mapping is shown in FIG. 4 by the solid and dashed lines between the logical DSP addresses 52 for DSPs 34 and 42 and the physical DRAM addresses. In mode 2, each DSP shares the entire 128K words of memory 54. In mode 2, either one of the lookup section 64 and 72 is independently mapped into the first logical section 56 of each DSP's memory range 52. Any one of the eight**

channel work areas 68 and 74 are independently mapped into the next logical 2k area 58 while any one of the eight channel areas 70, 76 are independently mapped into last logical 8k memory area 60", col. 8, line 52-62).

Regarding claims 2 and 3, a selector component in communication with mapping component and operable in a first selection mode to cause the mapping component to map based on the first map and operable in a second selection mode to map based on the second map **("Based on the inputs from register 36 and CAB1 TMML 38 will map the logical DSP addresses 52 of DSP 34 into the physical DRAM memory locations according to the maps shown in FIG. 4 and 5 for modes 1, 2 and 3, respectively. Similarly, based on the inputs from register 44 and CAB 2, TMML 46 will map the logical DSP addresses 52 of DSP 42 into the physical DRAM memory locations according to the maps shown in FIG. 4 and 5 for modes 1, 2 and 3, respectively." Col. 10, lines 20-30).**

Regarding claim 4, Andrews et al teaches wherein the selector component is further defined as a switch in communication with the mapping component, the switch having a first switch position associated with the first selection mode and a second switch position associated with the second selection mode **("multiplexer 40 connects the individual conductors in 41 and CDB2 to the corresponding individual conductors in the storage bus 50. This switching back and forth between busses**

39, CDB1 and 41 CDB2 is repeated over and over again in a continuing manner to storage bus 50"., see FIG. 3, element 40).

Allowable Subject Matter

4. Claims 6-12 are allowed over prior art made of record.

5. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 10/31/2008 have been fully considered but they are not persuasive. Applicant argues in Remark, page 10, that "Andrews fails to disclose or suggest physical channel corresponding to cabling wires." Applicant further argues "Andrews does not disclose, teach or suggest that the DSPs and the DRAM connect, use, or any way relate to cabling wires. Since Andrews does not disclose that the channels are connected to cabling wires or are associated with cabling wires, Applicant submits that claim 1 is allowable", page 12 of Remark.

Examiner respectfully disagrees because Andrews indeed teaches this arguable feature.

Andrews teaches a digital signal processing system includes two DSPs coupled to a data storage unit (see FIG. 5). Each of the DSPs 34 and 42 can perform complex digital signal processing algorithms such as, for example, CCITT spec V.32 (9600 bit/s

full duplex modems) and V.32 bits (14,400 bit/s full duplex modems) which require complex protocols and lookup intensive processing. Each of the DSPs 34 and 42 coupled to the data storage unit (DRAM) using T1 physical channel **("The first channel region includes four T1 channel areas"..."For mode 2 operation, the system of the present invention can process up to eight T1 channels")**. T1, which stands for Trunk Level 1 as digital transmission link with a total signaling speed of 1.544 Mbps. Therefore, Andrews indeed teaches the physical channels corresponding to cabling wires T1 Trunk.

Furthermore, Andrews teaches that each of the DSPs 34, 42 and the data storage unit are separate entities (see figure 5) and each of the digital processors (34 and 42) can independently access any of the memory location within the data storage unit (DRAM) via one of the eight physical channels (see FIG. 4). The terminology "Cable" may refer to a number of different types of wires or groups of wire capable of carrying voice or data transmissions. The physical channels, such as T1, coupled the digital processors to the data storage unit is indeed cable wires. Therefore, it is inherently a physical connection between the digital processors and the memory storage unit via a physical transmission medium, such as cable wires, in order for the DSPs to access any of the memory locations within the data storage unit.

Examiner respectfully believes Andrews et al teaches each and every limitation in the claim. Therefore rejection stands.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brenda Pham whose telephone number is (571) 272-3135. The examiner can normally be reached on Monday-Friday from 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

January 22, 2009

/Brenda Pham/

Primary Examiner, Art Unit 2416

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/816,738	BARMETTLER, MARK G.	
	Examiner	Art Unit	
	Brenda Pham	2416	